EXHIBIT 2

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571-272-7822

Paper 15
Entered: July 19, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00237
Patent 10,268,608 B2

Before JON M. JURGOVAN, NABEEL U. KHAN, and KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

KHAN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314, 37 C.F.R. § 42.4

I. INTRODUCTION

A. Background and Summary

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–5 ("the challenged claims") of U.S. Patent No. 10,268,608 B2 ("the '608 patent," Ex. 1001). The Petition challenges the patentability of claims 1–5 of the '608 patent. Netlist, Inc. ("Patent Owner") timely filed a Preliminary Response (Paper 12, "Prelim. Resp.").

An *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing on any of the challenged claims of the '608 patent. Accordingly, we do not institute an *inter partes* review as to the challenged claims of the '608 patent.

B. Related Proceedings

The parties identify the following matter as related to this case: *Netlist, Inc. v. Micron Technology, Inc., et al.*, Case No. 6:21-cv-00431-ADA (W.D. Tex.). Pet. 70; Paper 6, 1. Patent Owner states that matter was subsequently "transferred from the U.S. District Court for the Western District of Texas, Waco Division to the U.S. District Court for the Western District of Texas, Austin Division and docketed as" *Netlist, Inc. v. Micron Technology, Inc., et al.*, 1:22-cv-00136-LY (W.D. Tex.). Paper 6, 1.

Petitioner also identifies IPR2022-00236 as involving the parent of the '608 patent. Pet. 70. Petitioner further identifies IPR2017-00730 as involving a patent related to the '608 patent. *Id.*

C. The '608 Patent (Ex. 1001)

The '608 patent, titled "Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers," relates to a memory system which controls timing of memory signals based on timing information. Ex. 1001, codes (54), (57). Figure 2A, reproduced below, illustrates a memory module. *Id.* at 2:43–45, 4:65–66.

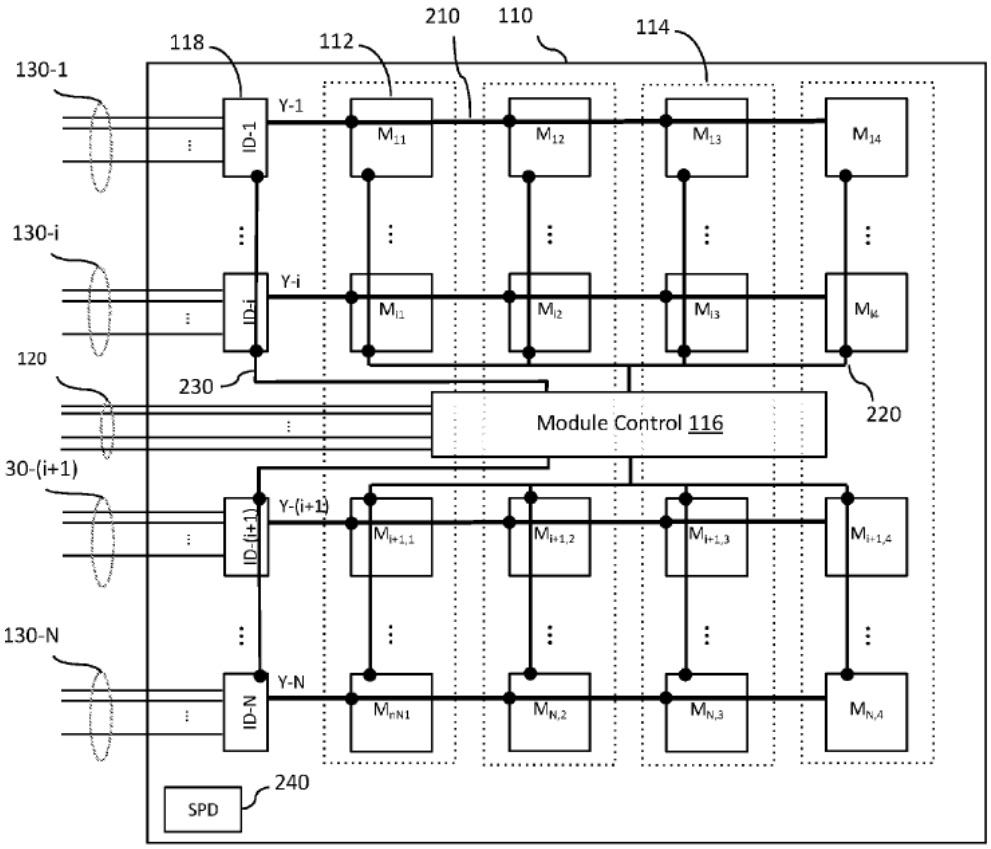

FIG. 2A

As shown in Figure 2A, memory module 110 includes module control device 116 and plurality of memory devices 112. Ex. 1001, 4:65–66, 6:4–5. Memory module 110 further includes control/address signal lines 120 and data/strobe signal lines 130, which are coupled to a memory controller

(MCH) (not shown). *Id.* at 4:20–23, 4:67–5:4. Respective groups of data/strobe signal lines 130 are also coupled to respective isolation devices, or buffers, 118, e.g., group of data/strobe signal lines 130-1 is coupled to isolation device ID-1. *Id.* at 4:23–25; *see id.* at 6:20–25. Furthermore, each isolation device 118 is associated with, and coupled to, a respective group of memory devices via module data/strobe lines 210. *Id.* at 6:17–20, 6:30–32. For example, as shown along the top of memory module 110, isolation device ID-1 "is associated with [a] first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices" via module data/strobe lines 210. *Id.* at 6:20–25.

In operation, memory module 110 "perform[s] memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.)." Ex. 1001, 3:29–32. Those commands are transmitted over control/address signal lines 120 and data/strobe signal lines 130 from the memory controller. *Id.* at 3:32–34, 4:66–5:3. For example, "[w]rite data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118." *Id.* at 7:63–65. And, "read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130." *Id.* at 7:66–8:3.

As can be seen in Figure 2A, and as the '608 patent explains, there are "unbalanced" lengths of control wires to respective memory devices which causes a "variation of the timing" of signals due to the variation in wire length. *See* Ex. 1001, 2:20–31; *see also id.* at 8:22–55. To account for timing issues, each isolation device, or data buffer, 118 is "responsible for providing a correct data timing" and "providing the correct control signal

timing." *Id.* at 8:56–9:3. In particular, "isolation devices 118 includes signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation." *Id.* at 15:23–26. For example, because write signals are received by isolation device 118, isolation device 118 uses that knowledge and determines timing information which is used to "properly time transmission" of a later read operation. *Id.* at 15:45–50.

D. Illustrative Claims

Claim 1, the sole independent claim of the '608 patent, is reproduced below with limitation identifiers in brackets corresponding to corresponding claim analysis headings in the Petition. *See* Pet. 20–41.

> 1. [a] A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
>
> [b] a module board having edge connections for coupling to respective signal lines in the memory bus;
>
> [c] a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and
>
> [d] memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, [e] the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

> [f] a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, [g] coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, [h] the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and [i] a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and [j] a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

Ex. 1001, 19:14–55.

E. Evidence

The Petition relies on the following references:

Reference	**Exhibit No.**
US 2010/0312925A1; filed June 3, 2010; published Dec. 9, 2010 ("Osanai").	1005
US 8,020,022B2; filed Sept. 12, 2008; issued Sept. 13, 2011 ("Tokuhiro").	1006
US 8,713,379B2; filed Nov. 22, 2011; issued Apr. 29, 2014 ("Takefman")	1007

Petitioner also relies on the Declaration of Donald Alpert, Ph.D. (Ex. 1003) in support of its arguments. The parties rely on other exhibits as discussed below.

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–5 would have been unpatentable on the following grounds:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1	1, 4	102[1]	Osanai
2	1–5	103(a)	Osanai, Tokuhiro
3	1–5	103(a)	Osanai, Tokuhiro, Takefman

II. ANALYSIS

A. Principles of Law

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")); *see also* 37 C.F.R. § 42.104(b) (requiring a petition for *inter partes* review to identify how the challenged claim is to be construed and where each element of the claim is found in the prior art patents or printed publications relied upon).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. Inc., v. Union Oil Co.*, 814 F.2d 628, 631 (Fed. Cir. 1987); *see also Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. Because the '608 patent claims priority before this date, the pre-AIA version of §§ 102 and 103 applies.

1323, 1334 (Fed. Cir. 2008) (to anticipate a patent claim under 35 U.S.C. § 102, "a single prior art reference must expressly or inherently disclose each claim limitation"). Moreover, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. § 102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Whether a reference anticipates is assessed from the perspective of one of ordinary skill in the art. *See Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368–69 (Fed. Cir. 2003) ("'[T]he dispositive question regarding anticipation [i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in that single reference." (second and third alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991))).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (internal quotation marks and citation omitted).

Petitioner's declarant, Dr. Alpert, opines that:

> a person of ordinary skill in the art in the field of the Challenged Patent would have been a person with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Such a person would have been knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers . . . an individual with additional education or additional industrial experience could still be of ordinary skill in the art if that additional aspect compensates for a deficit in one of the other aspects of the requirements stated above.

Ex. 1003 ¶ 42; *see* Pet. 5.

Patent Owner states that it "disputes Petitioners' definition of the level of a person of ordinary skill in the art," but does not present arguments in support of its assertion at this stage in the proceeding. Prelim. Resp. 11.

For purposes of this Decision, we adopt Petitioner's proposed level of ordinary skill, except that we find that the phrase "at least" in Petitioner's proposed definition creates a vague, open-ended upper bound for the level of ordinary skill, and we therefore do not adopt that aspect of the proposal. Thus, we determine at this stage of the proceeding, that a person of ordinary skill in the art would have been a person with an advanced degree in

electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and three years working in the field.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2020).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner proposes we "use Patent Owner's proposed constructions" from the related proceedings. Pet. 12; *see* Ex. 1019.

Patent Owner states that it "does not propose that the Board construe any claims." Prelim. Resp. 12.

We determine no terms need to be construed to resolve the disputes between the parties at this stage of the proceeding.

D. Anticipation by Osanai (Ground 1)

Petitioner argues claims 1 and 4 of the '608 patent are anticipated by Osanai. Pet. 20–45. Below we provide a brief overview of the prior art

references and then analyze Petitioner's contentions in light of Patent Owner's arguments.

1. Osanai (Ex. 1005)

Osanai relates to a memory module having memory chips and data register buffers arranged in a manner which shortens data line lengths. Ex. 1005, code (57). Figure 1, reproduced below, is a schematic diagram of a configuration of a memory module." *Id.* ¶ 20.

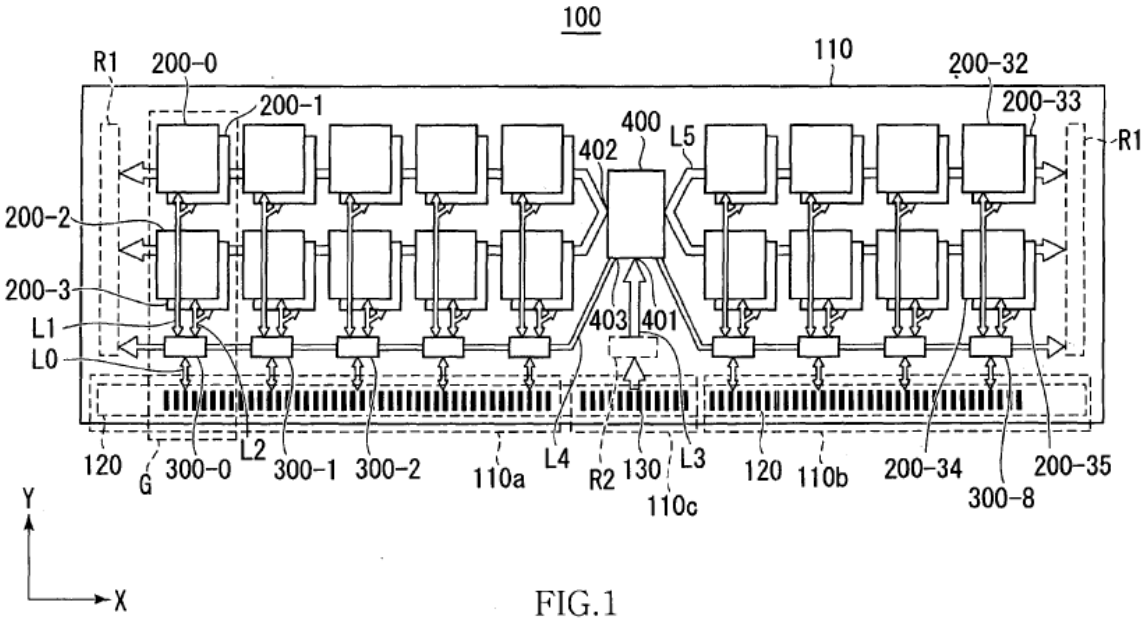

FIG.1

As shown in Figure 1, memory module 100 includes a plurality of memory chips 200 mounted on module substrate 110. *Id.* ¶ 51. Further, memory module 100 includes nine data register buffers 300-0 to 300-8 and address/control register buffer 400. *Id.* ¶ 52. Still further, memory module 100 includes "data connectors 120 [which] are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and [a] memory controller" ellectrically connected to the connectors. *Id.* ¶¶ 53–54 (memory controller not shown). As can be seen in Figure 1, and as further detailed in Figure 7, "data register buffer 300 intervenes between the data connectors

120 and the memory chips 200." *Id.* ¶ 109. Figure 7, reproduced below, is a connection diagram of memory module 100. *Id.* ¶ 26.

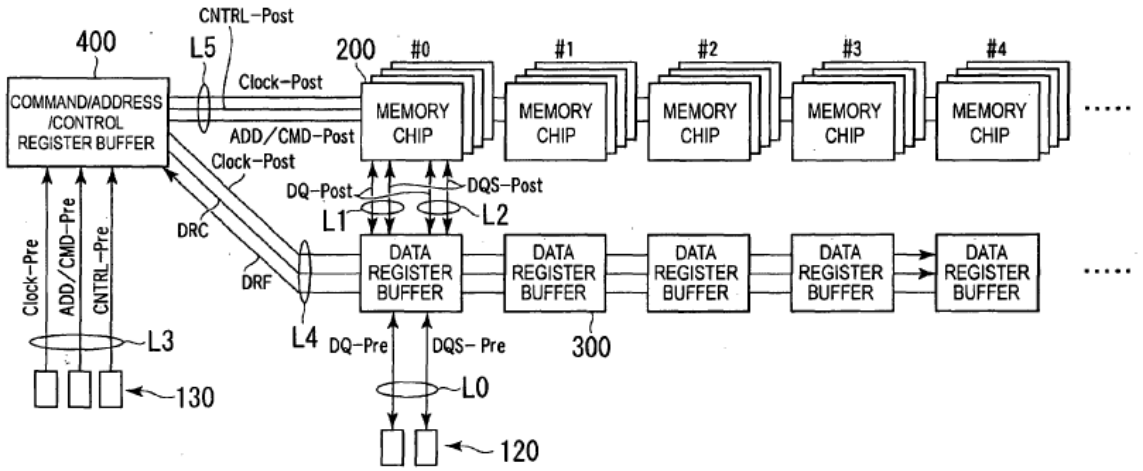

FIG.7

As shown in Figure 7, "data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2." Ex. 1005 ¶ 109. "[A] data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post." *Id.*

Further, "[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post." Ex. 1005 ¶ 110. As such, "it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller." *Id.* Osanai "adjust[s] a write timing or a read timing in consideration of a propagation time of a signal" via leveling operations. *Id.* ¶ 146. The write leveling and read leveling operations are provided via write leveling and

read leveling circuits in the data register buffer, as shown in Figure 5, which is a block diagram of the configuration of the data register buffer 300 and is reproduced below. *Id.* ¶ 89.

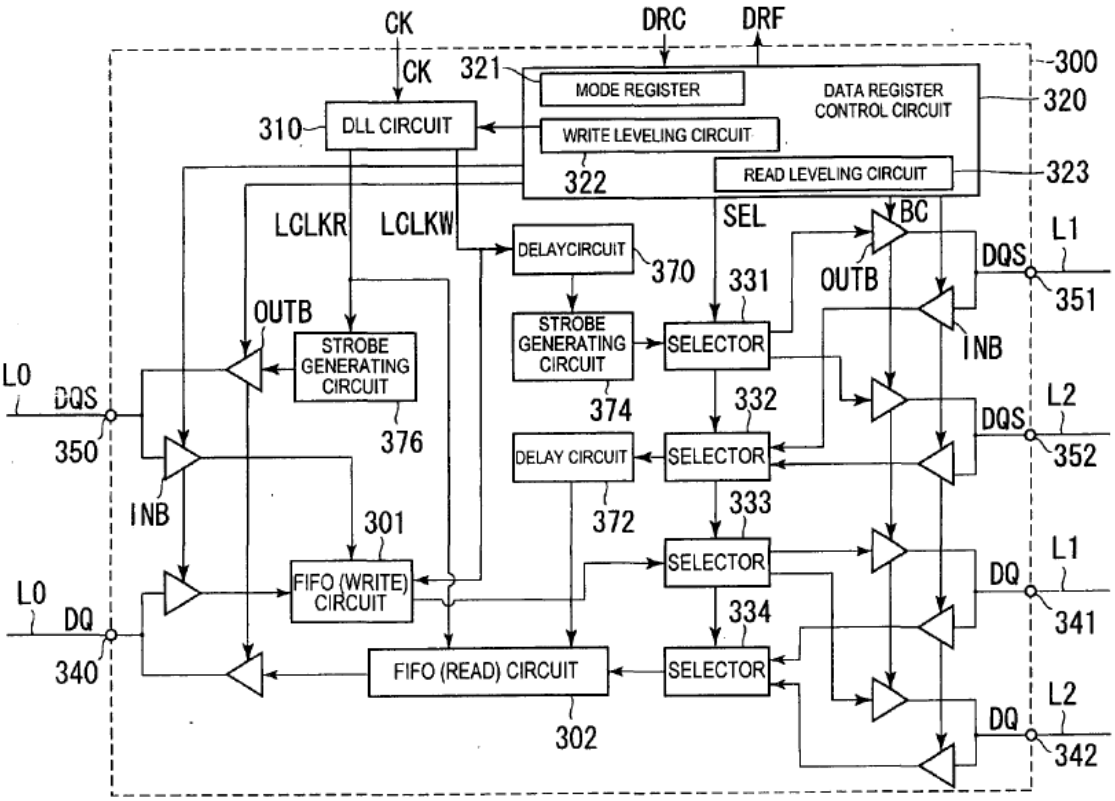

FIG.5

As shown in Figure 5, data register buffer 300 includes write leveling circuit 322 and read leveling circuit 323. Ex. 1005 ¶¶ 151, 153. The write leveling and read leveling operations "adjust a write timing or a read timing in consideration of a propagation time of a signal." *Id.* For example, in a write operation, "[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side." *Id.* ¶ 149. To compensate for that, "write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS." *Id.* ¶ 151.

An exemplary read leveling operation also adjusts signal timing for a read operation. *See* Ex. 1005 ¶¶ 153–157. For example,

> read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like.

Id. ¶ 157.

2. Analysis of Claim 1

a) Preamble and Undisputed Limitations 1[a]–1[i]

Petitioner provides detailed analysis demonstrating that Osanai discloses the preamble and limitations 1[b]–1[i]. Pet. 20–33. Petitioner supports its arguments with citations to Osanai and to the testimony of Dr. Alpert. *Id.* Patent Owner does not separately dispute Petitioner's contentions regarding the preamble and these limitations. At this stage of the proceeding, we are persuaded that Petitioner has demonstrated a reasonable likelihood that Osanai teaches the preamble and limitations 1[b]–1[i] for the reasons provided by Petitioner.

For example, for the preamble, Petitioner identifies Osanai's memory module 100 as the recited "memory module" and the memory control hub 12 as the recited "memory controller." Pet. 20 (citing Ex. 1005 ¶¶ 69–71). Petitioner argues that memory module 100 and control hub 12 communicate using line 23, which the Petitioner identifies as the recited "memory bus." *Id.* at 21–23 (citing Ex. 1005 ¶¶ 54–55, 75, Figs. 1, 3; Ex. 1003 ¶¶ 76–78). Petitioner argues that line 23 connects signal lines L0 and L3, which are the

recited "data/strobe signal lines" and "control/address signal lines," respectively. *Id.* at 24 (citing Ex. 1005 ¶¶ 54–55, 75; Ex. 1003 ¶ 80).

For limitation 1[b], Petitioner argues that Osanai's memory module 100 includes data connectors 120 and 130 which, together, disclose the recited "module board having edge connections." Pet. 24–25 (citing Ex. 1005 ¶ 54, Fig. 1; Ex. 1003 ¶ 83).

For limitation 1[c], Petitioner identifies command/address/control register buffer 400 as the recited "module control device mounted on the module board." Pet. 25–26 (citing Ex. 1005 ¶¶ 66, 101–103). Petitioner argues that Osanai's memory controller 12 sends command/address/control signals (the recited "system command signals") to register buffer 400 and in response the register buffer 400 outputs "module command signals" and "module control signals," such as ADD, CMD, CTRL, and CK signals as well as control signal DRC. *Id.* at 26 (citing Ex. 1005 ¶¶ 53, 102; Ex. 1003 ¶ 87). Petitioner further argues Osanai's register buffer 400 receives Clock-Pre Signal and outputs Clock-Post signal, which Petitioner argues are the recited "system clock signal" and "module clock signal" respectively. *Id.* at 28 (citing Ex. 1005 ¶ 114, Fig. 6–7; Ex. 1003 ¶¶ 89–90).

For limitation 1[d] Petitioner identifies Osanai's memory chips 200 as the recited "memory devices" and argues that they perform memory operations, such as read and write operations, as instructed by receiving CNTRL-Post signals and Clock-post signals, which Petitioner identifies as the recited "module command signals" and "clock signals" respectively. Pet. 29–30 (Ex. 1005 ¶¶ 60, 101–114, Figs. 6, 7; Ex. 1003 ¶ 93).

For limitation 1[e] Petitioner argues Osanai's memory chips 200 are grouped into sets making "a plurality of sets of memory devices," and each

group has its own respective set of data/strobe signal lines. Pet. 30–31 (citing Ex. 1003 ¶¶ 96–97; Ex. 1005 ¶¶ 58, 109, Figs. 5, 7).

For limitation 1[f] Petitioner identifies Osanai's data register buffers 300 mounted on memory module 100 as the recited "plurality of buffer circuits" and argues that the register buffers 300 are each paired with a set of the memory chips and L0 data lines. Pet. 31–33 (citing Ex. 1003 ¶¶ 100–101; Ex. 1005 ¶¶ 52, 61–62, 109, Figs. 1, 7).

For limitation 1[g] Petitioner argues that each data register buffer ("buffer circuit") is mounted on the module between L0 data lines ("data/strobe signal lines") and its respective memory chip group ("set of memory devices"). Pet. 33–34 (citing Ex. 1005 ¶ 109, Figs. 1, 7). Petitioner further argues that Osanai's command/address/control register buffer 400 ("module control device") outputs Clock-Post signal ("module clock signal") and DRC ("module control signals") to the buffer circuits 300. *Id.* at 34–35 (citing Ex. 1005 ¶¶ 93, 104, 112–114, 154, 157, 164, Figs. 6–7; Ex. 1003 ¶ 107).

For limitation 1[h] Petitioner argues that each data register buffer 300 has data paths that correspond to each data signal line L1 and L2, connected to each memory chip group. Pet. 36 (citing Ex. 1005 ¶ 109, Fig. 7). Petitioner argues that these data paths include circuitry components in the data register buffer 300 that connect each L0 data lines ("respective set of data/strobe signal lines"). *Id.* at 36–38 (citing Ex. 1003 ¶¶ 110–112; Ex. 1005 ¶ 109, Figs. 1, 5, 7).

For limitation 1[i] Petitioner identifies the data register control circuit 320 and DLL circuit 310 in the data register buffer 300 as the recited "command processing circuit" and argues that this circuitry uses the received DRC signals and clock signals to select the appropriate data path

("to control the data path in accordance with the module control signals and the module clock signal"). Pet. 38–40 (citing Ex. 1005, ¶¶ 94, 96, 97, 105, 132, 158, 163, Figs. 2, 5; Ex. 1003 ¶ 115). Petitioner further argues that any data path selected by Osanai's data register control circuit 320 includes a "tristate buffer" such as Osanai's OUTB buffers. *Id.* at 40–41 (citing Ex. 1005 ¶¶ 90–94, 97–98, 105–106, 129–136, Figs. 5, 11; Ex. 1003 ¶ 116).

b) Disputed limitation 1[j]

Petitioner argues that Osanai's control circuit 320 includes read leveling and write leveling circuits 322 and 323 and Dr. Alpert testifies that these circuits compensate for propagation delays caused by some memory chips being placed farther away from their respective data register buffers. Pet. 41–42 (citing Ex. 1005 ¶ 146, Fig. 5; Ex. 1003 ¶¶ 120–121). Petitioner argues that the write leveling circuitry 322 delays the output timing of the DQS sent from the data register buffer 300, thus creating DQS-Post and that the read leveling circuitry similarly delays signals. Pet. 43 (citing Ex. 1005 ¶¶ 151–157; Ex. 1003 ¶ 123). Petitioner argues that these delays were "in response to at least one of the module control signals" because the delays depend on whether the DRC mode represents a read operation or write operation and alternatively because read and write leveling circuitry uses the module clock signal. *Id.* at 44 (citing Ex. 1005 ¶¶ 94, 132, 154–157, 164, Fig. 7; Ex. 1003 ¶ 124).

Patent Owner argues that Petitioner fails to clearly identify any claimed delay circuit configured to delay a signal, arguing that although Petitioner makes remarks regarding Osanai's write leveling circuit and read leveling circuit, Petitioner never expressly identifies either as the recited "delay circuit." Prelim. Resp. 15. Patent Owner further argues that Petitioner fails to identify any data path that includes Osanai's write leveling

circuitry 322. *Id.* at 16. Patent Owner further argues that Petitioner does not identify a signal that is delayed through the recited data path. *Id.* at 17–19. Specifically, Patent Owner argues that Osanai's write leveling circuit 322 performs any delay before the DQS signals, which Petitioner relies on as the recited delayed signal, are even generated. *Id.* at 19. Patent Owner argues that "a signal cannot be '*delay[ed]*' as claimed unless it exists." *Id.* (alteration in original).

We do not agree with Petitioner's contentions. Specifically, we agree with Patent Owner that Petitioner has not identified a data path that includes Osanai's write leveling circuit 322. Claim 1 recites "wherein the data path . . . includes at least one tristate buffer . . . and a delay circuit configured to delay a signal through the data path." Thus, claim 1 requires that the data path include two elements: (1) at least one tristate buffer and (2) a delay circuit. We first examine Petitioner's contentions with respect to the "data path" limitation and then analyze whether Petitioner has sufficiently identified a delay circuit that is included in the aforementioned data path.

With respect to the "data path," Petitioner argues that "each data register buffer 300 has '*data paths*' that correspond to each data signal line, L1 and L2 data lines, connected to each memory chip group." Pet. 36 (citing Ex. 1005 ¶ 109, Fig. 7). Petitioner argues that "these data paths include circuitry components in the data register buffer 300 that connect each L0 data lines ('*respective set of data/strobe signal lines*') at terminals 340 and 350." Pet. 36–38 (citing Ex. 1003 ¶¶ 110–112; Ex. 1005 ¶ 109, Figs. 1, 5, 7). Initially, we note, that while Petitioner states that data register buffer 300 has data path***s***, Petitioner does not, even by way of example, identify any single one of those data paths as disclosing the recited "data path." Moreover, Petitioner does not specifically identify which circuitry

components of data register buffer 300 are included in any one of the data paths cited by Petitioner.

With respect to the "delay circuit" Petitioner identifies Osanai's write level circuitry 322 and read leveling circuitry 323[2] and argues that the write level circuitry 322 delays the output timing of the DQS sent from the data register buffer 300, thus creating DQS-Post and that the read leveling circuitry similarly delays signals. Pet. 43 (citing Ex. 1005 ¶¶ 151–157; Ex. 1003 ¶ 123). Petitioner does not, however, state, or otherwise make a showing, that the write and read leveling circuitry are included in any one of the data paths that are relied upon by Petitioner. Nor does Petitioner show how these circuits would be included in the recited data path.

In contrast, with respect to the "tristate buffer," Petitioner explicitly states that "[a]ny data path selected by Osanai's data register control circuit 320 includes a 'tristate buffer'" and identifies Osanai's OUTB buffers as disclosing these tristate buffers. Pet. 40 (citing Ex. 1005 ¶ 94, Fig. 5; 1003 ¶ 116). Petitioner, however, does not make a similar statement regarding the delay circuit being included in the data path. Instead Petitioner contends that the "buffer circuits 300 include 'a delay circuit . . . .' *Id.* at 41. The claim, however, requires more than just the buffer circuit include the delay circuit. The claim requires the *data path* include the delay circuit. Based on our

[2] Patent Owner argues that Petitioner does not clearly and expressly identify any claimed delay circuit configured to delay a signal. Prelim. Resp. 15. We determine, however, that Petitioner relies on Osanai's write leveling circuitry 322 and read leveling circuitry 323 as disclosing the recited "delay circuit." *See* Pet. 43 (stating that the write and read leveling circuitry as the components that "delay a signal through the data path by an amount determined by the command processing circuit.")

review of Petitioner's contentions it appears Petitioner does not demonstrate this to be the case.

3. Conclusion – Anticipation by Osanai (Ground 1)

Accordingly, having considered the arguments and evidence, we are not persuaded that Petitioner has demonstrated a reasonable likelihood that Osanai anticipates claim 1, or claim 4, which depends from claim 1.

E. Obviousness over Osanai and Tokuhiro (Ground 2) and Obviousness over Osanai, Tokuhiro, and Takefman (Ground 3)

Petitioner argues claims 1–5 of the '608 patent would have been obvious over Osanai and Tokuhiro (Pet. 45–61) and over Osanai, Tokuhiro, and Takefman (Pet. 62–65). Petitioner relies on Tokuhiro for independent claim 1 as disclosing "delay[ing] a signal through the data path by an amount determined . . . in response to . . . control signals." *Id.* at 45–52. Petitioner relies on Takefman as disclosing the recited "tristate buffer." *Id.* at 62–65. Petitioner's contentions regarding Tokuhiro or Takefman do not address or remedy the deficiencies discussed above with respect to Ground 1.[3] Specifically, Petitioner does not rely on Tokuhiro or Takefman as disclosing that the delay circuit is included in the recited data path, as required by claim 1.

Claims 2–5 depend from claim 1. Accordingly, having considered the arguments and evidence, we are not persuaded that Petitioner has

[3] As with Ground 1, Petitioner recognizes in Ground 3 that claim 1 requires the recited "tristate buffer" to be included in the recited "data path" and, accordingly, provides reasoning why Takefman's tristate buffer would have been incorporated into Osanai's data paths. *See* Pet. 62–63. Petitioner does not recognize, or at least does not address, that claim 1 also requires the same of the recited "delay circuit" and thus does not address whether the relied upon references teach a delay circuit that is included in the recited data path.

demonstrated a reasonable likelihood that claims 1–5 would have been obvious over Osanai and Tokuhiro or would have been obvious over Osanai, Tokuhiro, and Takefman.

III. CONCLUSION

Petitioner has not demonstrated a reasonable likelihood of prevailing in showing the unpatentability of the challenged claims of the '608 patent.

IV. ORDER

For the foregoing reasons, it is

ORDERED that the Petition is *denied*, and no trial is instituted.

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